Self-Alignment Structures For Heterogeneous 3D Integration

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Abstract

A novel self-alignment technology, called positive self-alignment structures (PSAS), for heterogeneous 3D integration is described. Using a set of precisely reflowed photoresist structures in conjunction with the corresponding inverse pyramid pits, we demonstrate that submicron alignment can be achieved without an advanced placement tool. The *positive* self-alignment structure technology is fabricated on top of electronics or devices, and as a result, it does not take up additional electronic real estate, and it can be fabricated on any surface, including glass. This enables heterogeneous integration that involves non-silicon substrates, and at the same time simplifies the stacking of three or more chips. This paper describes the self-alignment mechanism, the fabrication of positive self-alignment structures (PSAS), and the test structures to measure the accuracy of alignment; the resulting misalignment on various substrates including glass and unpolished silicon surfaces are reported. In addition, the stacking of five chips is demonstrated and the resulting misalignment at each of the chip-to-chip interfaces is measured and reported.

Introduction

The ability to align and stack chips that are made of two dissimilar substrates is critical for future heterogeneous systems containing not just electronics but also optical and MEMS/sensor devices. Although, many of the optical [1] and MEMS/sensors [2] technologies are monolithically fabricated on silicon substrates, the presence of CMOS electronics in the same silicon substrate limits the materials and processes that can be used to fabricate these devices [3]. However, fabricating the CMOS electronics and non-CMOS devices independently on different substrates and stacking them on top of each other lifts the material and process constraints and allows one to optimize CMOS and non-CMOS technologies separately.

In 3D integration, the accuracy of the alignment between stacked components is critical because it significantly affects the performance of interconnects between stacked chips. For example, in optical interconnects, it is known that the alignment accuracy between two optically coupled chips is directly correlated to the coupling efficiency; it has been shown that for an optical system with silicon micro-mirrors, a submicron alignment accuracy is needed to achieve less than 3dB of optical loss and a bit error rate (BER) below 10^{-12} [4]. Another study that used grating couplers to improve the misalignment tolerance still resulted in 1dB excess loss for a 2 μm misalignment [5]. The misalignment is also known to negatively impact SNR of capacitive and inductive coupled interconnect [6].

In addition, the ability to control the gap between stacked chips plays an important role in improving the coupling efficiency. Specifically, in capacitive coupled proximity communication, the reduction of the gap can increase the capacitance between the pads, which improves the BER; 10 μm gap resulted in BER of 10^{-9}, while 11.5 μm gap increased the BER to 10^{-4}[6].

Despite the need for an accurate alignment, it is also desirable to align and assemble/stack two chips accurately

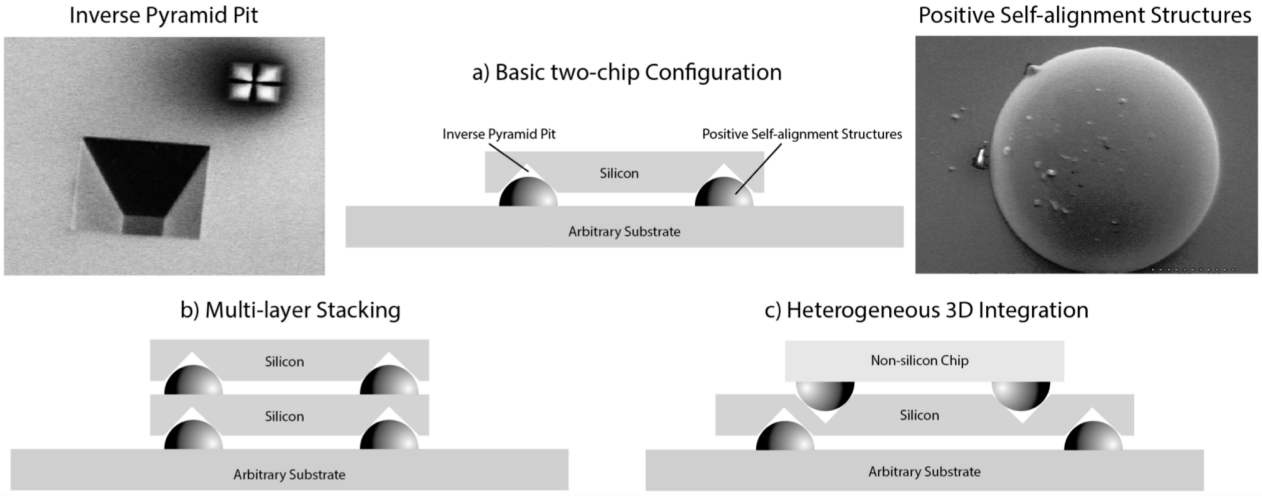


Figure 1. Configurations possible with positive self-alignment structures (PSAS) and inverse pyramid pits.

without the aid of an expensive assembly tool. This reduces packaging cost, and more importantly, it also opens up possibility for new packaging concepts.

In this paper, a self-alignment mechanism for accurately aligning two or more tiers (i.e. chips) without any alignment equipment is presented. The mechanism involves the fabrication of two types of structures; a positive structure is fabricated on one tier, and a negative trench structure is formed on the second tier.

After the fabrication of the two structures, the alignment is performed without the aid of a placement tool; first, the chips are brought together closely, and once the positive structure and the corresponding negative structure overlap slightly, some pressure is applied to automatically guide the positive structure to the center of corresponding negative structure (Figure 1). The gap between the chips is controlled by precisely controlling the dimensions of the two structures.

In addition, this paper reports alignment accuracy achieved by PSAS fabricated on various substrates including glass and unpolished silicon surfaces. Finally, the stacking of five chips is demonstrated and the resulting misalignment at each chip-to-chip interface is measured and reported.

Overview of the Self-alignment Mechanism

As described in the previous section, two types of structures are needed for the operation of the self-alignment mechanism described in this paper. The first structure is called the *positive* self-alignment structure (PSAS), which is an extruding surface micro-fabricated structure, as shown in Figure 1. The second structure is an inverse pyramid pit etched in the silicon substrate, which is also shown in Figure 1.

In the simplest form, the self-alignment mechanism can be used to align one silicon chip to an arbitrary substrate as shown in the two-chip configuration (Figure 1a). In this configuration, one of the chips would have either three or four PSAS spread out and placed in the overlapping regions of the substrate, while another chip (silicon) would have the inverse pyramid pits etched to the corresponding locations.

When these two substrates are initially brought together with a coarse alignment, and pressure is applied vertically, the PSAS are steered into the center of the corresponding pits, relatively aligning the two substrates more accurately.

Some of the key benefits of the novel PSAS include: first, the PSAS can be fabricated on any surface in which photolithography can be performed. This implies that PSAS can be fabricated not only on silicon wafers, but also on non-silicon substrates such as Pyrex and quartz (Figure 1c).

Second, the PSAS does not damage the surface underneath the structure. This means that electronics can be located directly underneath the PSAS structure so that silicon real estate is not wasted; the pit, which does take up electronics real estate, can be fabricated on the back side of the silicon wafer.

Finally, the PSAS does not involve other moving parts and can be processed at the wafer level before chips are diced. This lends itself to simpler 3D stacking without involving additional processes or tools.

Geometrical Considerations

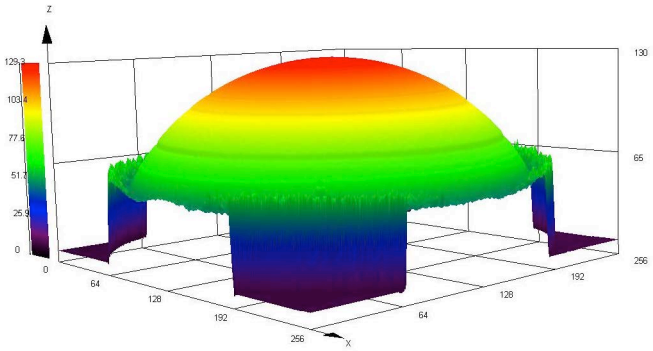
Not only does the geometry of both the PSAS and the pit play crucial roles in the self-alignment mechanism, but their dimensions must be carefully controlled. This section explores the effect of PSAS shape and dimensions on alignment accuracy.

Shape of PSAS

The shape of a reflowed structure can be determined using various ways [8]. In this work, the shape of the PSAS was approximated as a truncated sphere. In order to verify that this assumption is a valid one, a PSAS was scanned using a confocal laser microscope. The profile measured through the center of the PSAS is shown in Figure 2. The results demonstrate the following:

1. Profile scan through the center can be approximated as a circular segment, and
2. PSAS is radially symmetric as shown by the same horizontal and vertical profilometer scans.

a)



b)

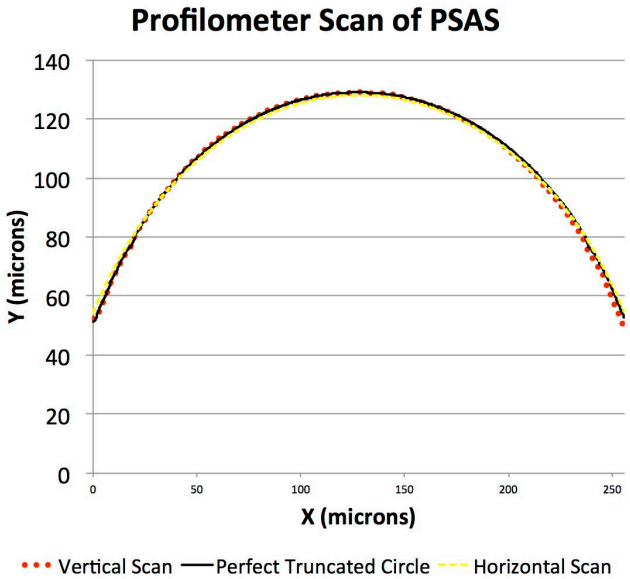


Figure 2. a) 3D image of PSAS scanned by the confocal laser microscope b) Plot showing the measured profile of the PSAS through the center point. Also plotted is a perfect truncated circle with a radius of 148 µm.

From the results, it is possible to conclude that the PSAS can accurately be represented and approximated as a truncated sphere.

PSAS and Pit Dimensions

The width of the pit is an important dimension that determines the maximum initial misalignment tolerated for the self-alignment mechanism to work. The initial coarse alignment tolerance is equal to half the width of the pit; initial alignment within this tolerance will place the center of the PSAS inside the pit, which will slide into the center of the pit when pressure is applied. To enable one to align chips without a placement tool, it is advantageous to make the coarse alignment tolerance as large as possible. In this paper, the pit was fabricated with 300 µm sides, which was large enough for chip assembly without an advanced placement tool.

The width of the pit, in conjunction with the diameter of the base of the PSAS, plays an important role in determining the gap between the two substrates that are being aligned.

Figure 3 represents the simplified geometry involved in the self-alignment mechanism and the gap between the substrates can be derived as shown below. The triangle represents the cross-section of the inverse pyramid pit; ***α***, is the {111} planes in the silicon crystal, which is at an angle of 54.7 degrees, and therefore, making ***β*** to be 35.3 degrees. The semi-circle and the circle segment represent the PSAS; ***g*** is the gap between the two chips, and ***h*** is the distance from the top chip surface to the imaginary center of the sphere. If the PSAS is a semi-sphere, then ***g*** will be identical to ***h***, and ***t***, which is the difference between ***h*** and ***g,*** would be zero.

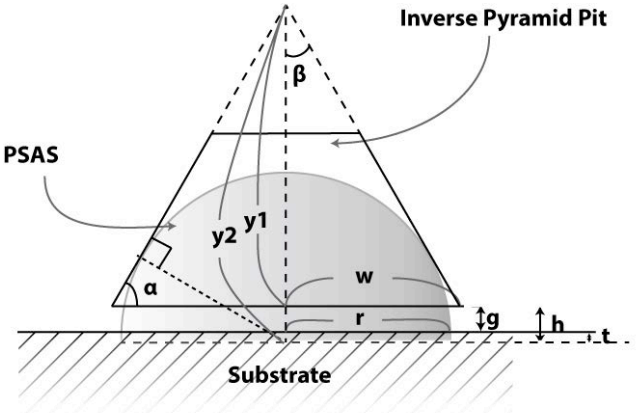


Figure 3. Geometry involved in the self-alignment mechanism.

The pit depth, y_1, can be calculated using simple geometrical considerations, as shown below. ***w*** is the half the side width of the pit.

$$tan(\beta) = \frac{w}{y_1}$$
$$y_1 = \frac{w}{tan(\beta)} \quad (1)$$

Similarly, y_2 can be calculated as

$$sin\beta = \frac{r}{y_2}$$
$$y_2 = \frac{r}{sin\beta} \quad (2)$$

As a result, ***h*** and ***g*** can be derived as,

$$h = y_2 - y_1$$
$$h = \frac{r}{sin\beta} - \frac{w}{tan(\beta)}$$
$$g = h - t$$
$$g = \frac{r}{sin\beta} - \frac{w}{tan(\beta)} - t \quad (3)$$

The derived equations (3) show that the gap is dependent on both the pit width and the PSAS radius. Figure 4 illustrates the predicted gap as a function of the pit width.

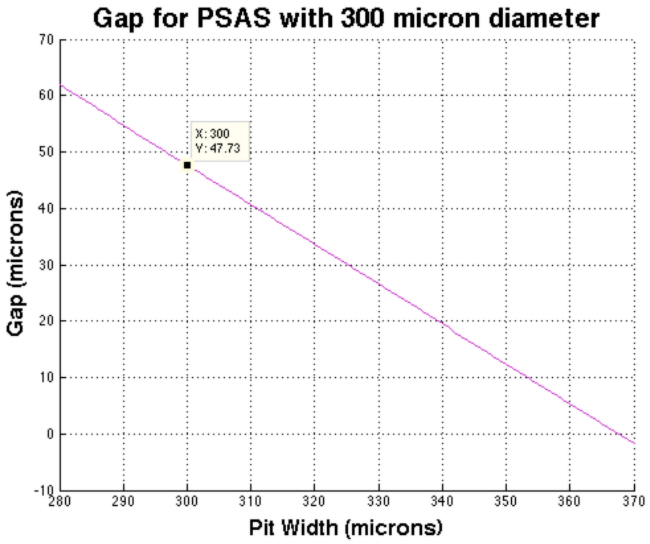


Figure 4. For a fixed PSAS diameter, the gap is dependent on the opening size of the pit. The graph is plotted for a semi-sphere PSAS (i.e. ***t=0***).

The ability to control the gap between substrates is critical in many applications. For example, in [9], the optical coupling efficiency is shown to be dependent on the gap; maximum coupling efficiency is achieved when the gap between the substrates is minimized.

In this paper, a PSAS of 150 µm radius and 130 µm tall is used. From Figure 4, a semi-sphere PSAS with 150 µm radius is predicted to have 48 µm of gap. For a 130 µm truncated sphere (i.e. ***t*** is 20 µm*)*, the expected gap is 28 µm.

Experiment Setup for Alignment Accuracy Measurement

To measure the relative alignment accuracy achieved using PSAS, two sets of chips were created. As shown in Figure 5, the first chip, a silicon chip, contains a vernier scale pattern and four pits etched on each corner. The second chip contains a corresponding vernier scale pattern and four PSAS

in the corresponding positions. When the two substrates are aligned, the overlay of the two patterns can be observed using an optical microscope (for transparent substrate) or an infrared microscope (for opaque substrate) to measure the misalignment in both the X and the Y directions at four corners of the chip.

The smallest misalignment that can be measured using the vernier pattern is 1 µm, which is the CD of the mask used in this experiment. The dimensions of the chips used in this experiment are 2 cm x 2 cm.

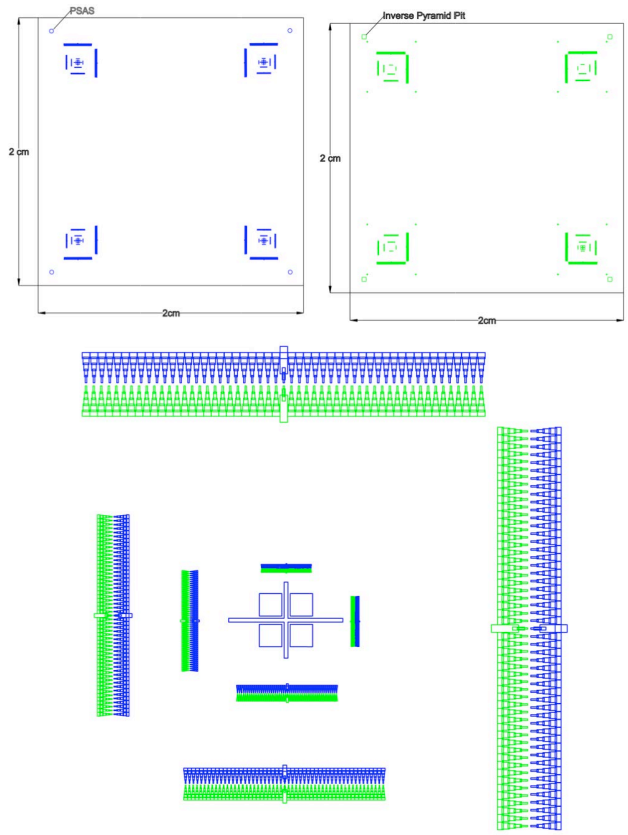


Figure 5. Mask layout used for the assembly experiment contains two sets of corresponding vernier scale patterns (one on each chip) designed to measure the relative alignment accuracy.

Fabrication Process

The alignment accuracy is strongly dependent on the ability to fabricate structures as close to the design as possible. Therefore, it is important to control the resulting dimensions of the PSAS and the pit very precisely.

Precision Reflow Process

The PSAS is fabricated by reflowing photoresist, which is a technique commonly used to make micro-lens arrays. To completely reflow a large photoresist structure, like PSAS, the reflow temperature must be high. This is because the time in which the photoresist remains glassy at an elevated temperature is limited by the increase in the glass-transition temperature during the reflow process [10]; at low temperatures, the glass transition temperature is raised above the reflow temperature before the photoresist is completely reflowed. However, high temperature causes the photoresist to reflow beyond the original pattern and results in a shape that is vastly different from the intended design. The work by Yang *et al.* has shown that by using temperature ramping even large structures can be reflowed completely without spreading [10]. The same techniques have been used in this paper.

Inverse Pyramid Pits

Inverse pyramid pits are fabricated using a chemical wet etch commonly used to make bulk micro-machined MEMS devices. KOH solution was used to anisotropically etch the [100] silicon wafer. Alternatively, TMAH, a CMOS compatible solution, can be used, if it is to be fabricated as a post-CMOS process [11].

Vernier Scale Patterns

Vernier scale patterns on the chip containing PSAS were fabricated using a lift-off process. The process begins with a silicon dioxide layer deposited on a blank wafer using a PECVD tool. Next, a negative resist (NR71-3000PY) is patterned, which contains the vernier scale pattern as well as a circular pattern where PSAS is to be located. Next, 300 angstroms of titanium is deposited using an e-beam evaporator. Finally, the negative resist is removed by submerging the wafer in acetone placed inside an ultrasonic bath.

To form PSAS, MicroChemicals photoresist is first spin coated and then patterned to form a cylinder with a height of 80 µm (Figure 6). Finally, using the precision reflow process described previously, 130 µm tall PSAS are formed (Figure 7).

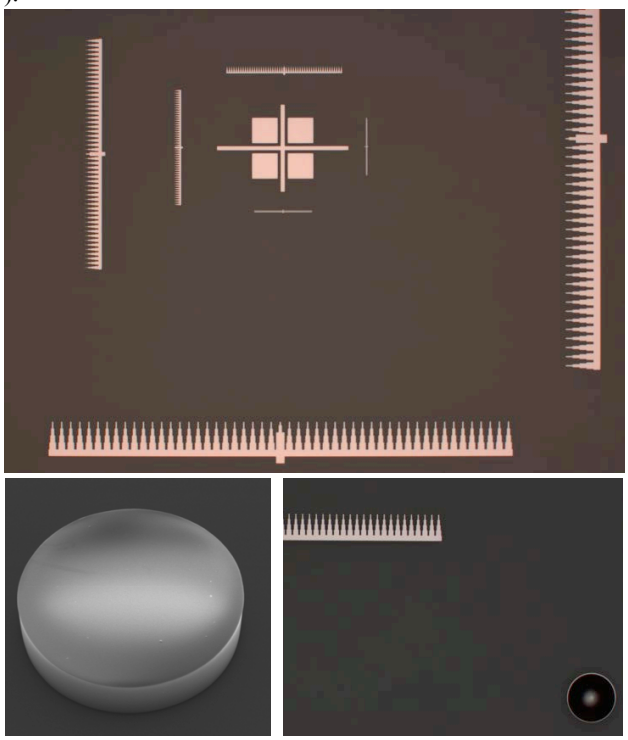


Figure 6. Optical and SEM images showing the vernier scale (top), photoresist before reflow (left), and vernier scale pattern and reflowed photoresist (right).

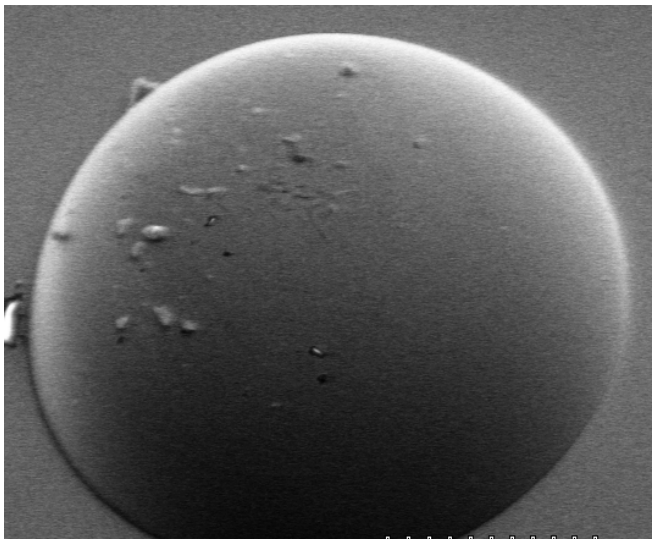


Figure 7. SEM image of a positive self-alignment structure.

Vernier patterns on the chip containing the inverse pyramid pits were fabricated at the same time as the pits to minimize the misalignment during the patterning process. First, a thermal oxide is grown in LPCVD. Next, the vernier scales and the square openings for the inverse pyramid pit are patterned. The wafer is then etched in a temperature controlled KOH solution, which etches the silicon pit and the vernier scales simultaneously. The square openings form the inverse pyramid pits, while the vernier patterns become suspended on top of a trench, as shown in Figure 8. The suspended structures were sturdy enough for the measurement in subsequent sections.

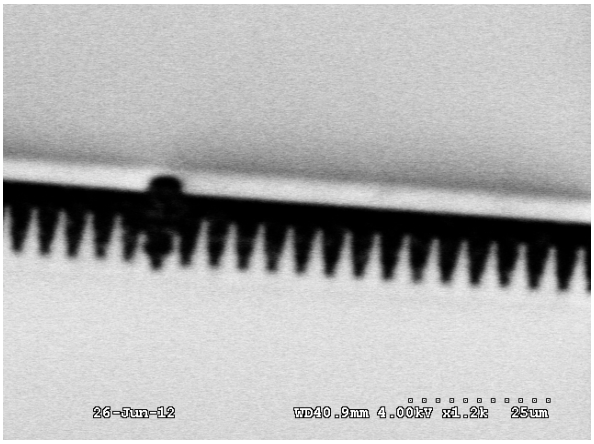


Figure 8. SEM image showing vernier scale patterns fabricated at the same time as the inverse pyramid pit.

Alignment Accuracy Measurement

In this section, the alignment accuracy results are reported. After two substrates are brought together and self-alignment is induced, the vernier scale patterns were observed using either an optical microscope or an infrared microscope.

Heterogeneous Integration

The measurement of the alignment accuracy between a silicon chip and a glass chip was done using an optical microscope. An example of the optical image seen by an optical microscope is shown in Figure 9.

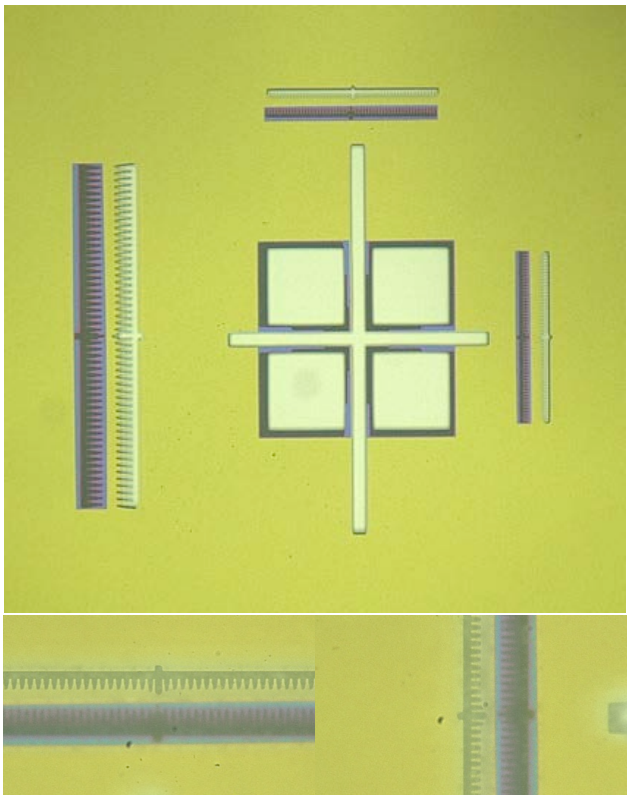


Figure 9. Optical microscope image showing the overlay of the two vernier scale patterns. Bottom images show high magnification images of the smallest vernier patterns.

The alignment accuracy between two polished silicon chips was measured by an infrared microscope, which allows one to see patterns that are placed between two opaque silicon substrates. An example of an image shown by the infrared microscope is shown in Figure 10.

The alignment accuracy between a polished silicon chip and an unpolished silicon chip was also measured with an infrared microscope. However, because of the surface roughness, the vernier patterns were not clearly visible making it difficult for an accurate measurement. As a result, other large features of known sizes were used to determine the accuracy. The limit of the alignment accuracy that can be measured using this method was approximately 5 μm. An example of such image is shown in Figure 11.

Table 1 shows the alignment accuracy measured for PSAS fabricated on various substrate surfaces; it is worth noting that in most cases, the degree of misalignment is within the minimum misalignment discernable of the measurement technique.

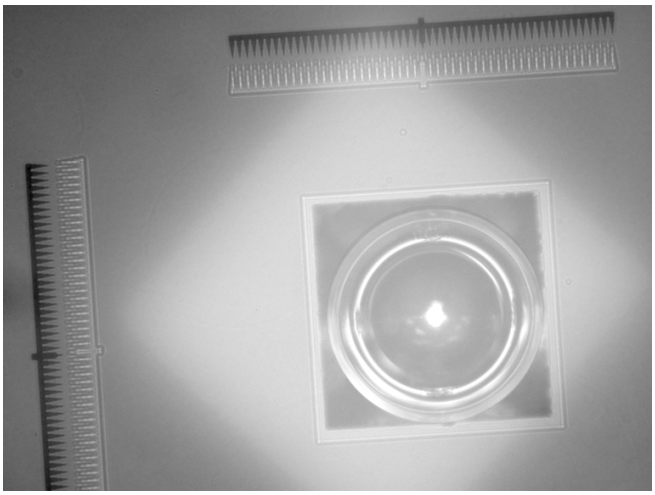


Figure 10. Vernier patterns on two silicon substrates can be imaged using an infrared microscope. The pit and the PSAS are also visible in this image.

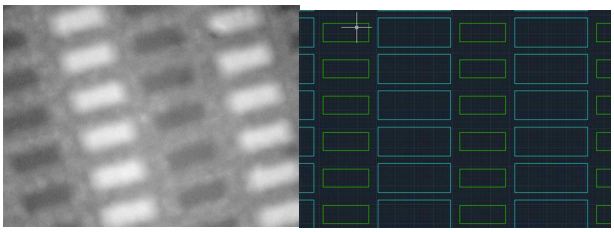


Figure 11. Unpolished silicon substrate makes it difficult to discern small features. Therefore, large features with a known dimensions were used to measure alignment accuracies. Left image shows the infrared microscope image and the right image shows the corresponding section in the original layout.

Table 1. Alignment Accuracy Achieved by PSAS on Various Substrate Surfaces

(in microns)

Substrate	*Left Top X,Y*	*Right Top X,Y*	*Left Bottom X,Y*	*Right Bottom X,Y*
Glass	*1,6*	*1,6*	*<1,1*	*1,<1*
Unpolished Silicon	*<5*	*<5*	*<5*	*<5*
Polished Silicon	*<1.<1*	*<1,<1*	*<1,<1*	*1,1*

Stacking of Multiple Chips

As mentioned above, PSAS can be used to stack more than two chips. Figure 12 illustrates a stack of five chips assembled without a placement tool. The PSAS and the inverse pyramid pits in the chips were fabricated similarly to the ones described in the previous section. However, the pit and the PSAS were fabricated in the same wafer, and the front- and back-side vernier patterns were aligned using a back-side mask alignment tool. As seen from the results in Table 2, this introduced misalignment independent of the performance of PSAS (i.e., this is purely dictated by the lithography tool).

The alignment accuracy between the different surfaces in the stack of five chips can also be measured using an infrared microscope by focusing on various surfaces. However, as the focus is changed to discern features in lower surfaces, the image fidelity and contrast degraded significantly; though it was possible to see the vernier patterns clearly in the first 3 chips i.e. (surfaces 1-6 in Figure 13), the last two chips (i.e. the surfaces 7-10 in Figure 13) were not clear enough for measurements. To obtain results for the last two surfaces, the stack was flipped upside down and the alignment accuracy was measured using the same method as the first 6 surfaces.

The smallest vernier patterns, which were designed to discern misalignments in the range of 1 to 5 μm were not visible for the stack of 5 chips using the infrared microscope. As a result, the larger vernier scale patterns were used, which increased the minimum alignment accuracy that can be measured from 1 μm to 5 μm.

Once the images focused on various surfaces were captured, the images were overlaid on top of each other using an image processing software. This enabled one to see both sets of vernier patterns (located on different surfaces) at the same time. This is critical as this enabled visual discerning of the relative position of the scales for measuring alignment accuracy.

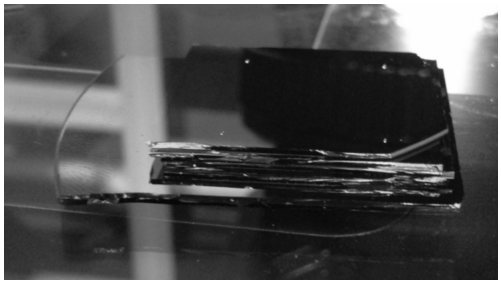


Figure 12. Image showing five chips aligned and stacked using PSAS, without the using a placement tool.

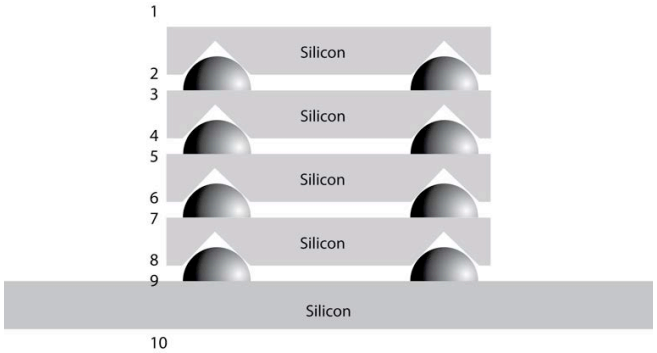


Figure 13. A schematic denoting the number of each surface within a five-chip stack.

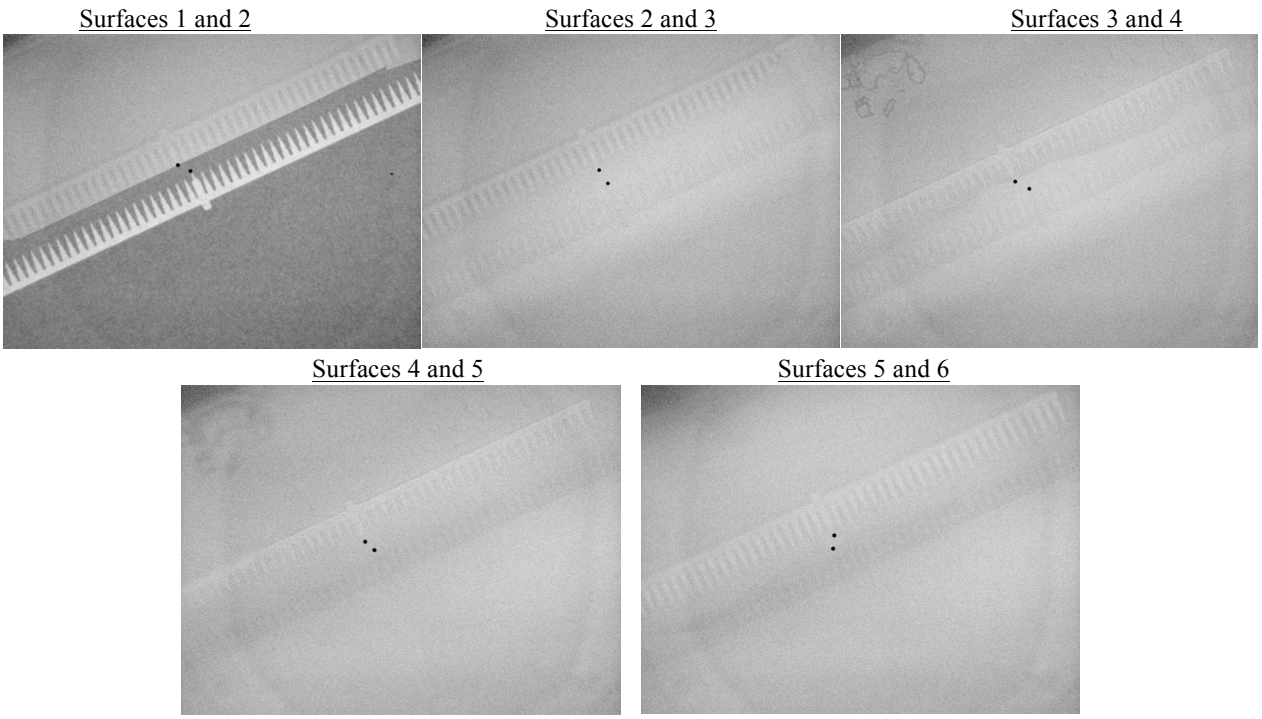


Figure 14. Infrared images of the surfaces overlaid on top of each other using an image processing software. The overlaid image allows one to determine the misalignment between surfaces easily. The black dot represents the center tip of the vernier scale pattern. This figure shows images for the X direction.

Table 2. Magnitude of Misalignment by Surface Interface

(* surfaces were observed by flipping the stack)

Between Surfaces	*Misalignment* *X*	*Y* (*μm*)	*Alignment Method*
1 and 2	10	0-5	Backside Alignment
2 and 3	0-5	0-5	PSAS
3 and 4	11	0-5	Backside Alignment
4 and 5	5	0-5	PSAS
5 and 6	8	0-5	Backside Alignment
6 and 7*	0-5	0-5	PSAS
7 and 8*	8	0-5	Backside Alignment
8 and 9*	0-5	0-5	PSAS

Table 3. Magnitude of Misalignment by Chip

(* surfaces were observed by flipping the stack)

Between Chips	*Misalignment* *X*	*Y* (*μm*)
Chip 1 (top) and 2	0-5	0-5
Chip 2 and 3	5	0-5
Chip 3 and 4*	0-5	0-5
Chip 4 and 5 (bottom)*	0-5	0-5

As seen from the results in Table 2, the major misalignment is from the back-side alignment tool. On the other hand, the misalignment from PSAS (Table 2 and Table 3) is below or at the minimum resolution of this technique, which is 5 μm. This result is also consistent throughout the stack, demonstrating the repeatability of accurate heterogeneous chip-to-chip alignment using PSAS.

Conclusions

In this paper, a novel method of aligning chips has been demonstrated. Using positive self-alignment structures (PSAS), submicron alignment accuracy can be achieved between a silicon chip and an arbitrary chip, without using a placement tool. PSAS can also be used to stack multiple chips, and 5 μm alignment accuracy has been demonstrated between stacked chips.

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